FORM PTO 1449 (*modified*)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT(S)
(Use several sheets if necessary)

ATTY DOCKET NO.	APPLICATION NO.
NL031031US1	10/570,290

APPLICANT: Adrianus Josephus Bink, et al.

FILING DATE	GROUP
February 28, 2008	2185

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,666,482	9/9/1997	McClure			
		5,958,068	9/28/1999	Arimilli, et al.			
		2001/0039601	11/8/2001	Leung et al.			
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OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)

/M.G./		Yamashita, K. et al. "A Design and Yield Evaluation Technique for Wafer-Scale Memory", Computer, vol. 25, issue 4, pgs. 19-27 (4/1992)
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/M.G./		International Preliminary Report on Patentability for Int'l. Patent Appln. No. PCT/IB2004/51465 (March 6, 2006)

EXAMINER	DATE CONSIDERED
/Mark Giardino Jr/	06/21/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.G./